ANALOG DEVICES

AN-662
APPLICATION NOTE

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Input Leakage Current in High Speed Applications

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INTRODUCTION

This application note examines the input currents found on high speed Σ-Δ ADCs due to multiplexing, system chopping, and the load presented by an unbuffered Σ-Δ modulator. While the AD7738 and AD7739 are the main focus of this application note, it should be relevant to any high speed data acquisition system.

The AD7738 and AD7739 feature on-chip buffers with input leakage specifications of 200 nA (AD7738) and 5 nA (AD7739). Without these buffers, the user would be exposed to the load presented by an unbuffered Σ-Δ. However, even with these buffers, there are other input currents caused by channel changing and system chopping.

A block diagram to illustrate the AD7739 front end is shown below. The front end consists of a 9-channel multiplexer with inputs AIN0 to AIN7 and a common pin. The nine analog inputs may be configured as eight pseudo differential, four fully differential, or a mixture of pseudo differential and fully differential.

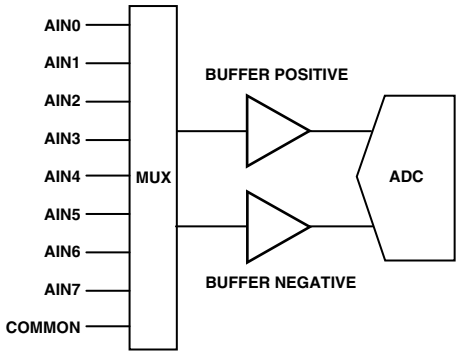

Figure 1. AD7739 Front End

The multiplexer output is made available off chip on the AD7738 (Pins MUXP, MUXN and ADCP, ADCN) but on the AD7739 is not pinned out to reduce the multiplexer output capacitance.

CURRENTS DUE TO MULTIPLEXING

In Figure 2, see a simplified drawing of a multiplexed input consisting of two inputs, one of which is at V_1 = 1.25 V and the other at V_2 = 3.75 V. On the multiplexer output is a capacitor C_{LOAD}. The capacitance C_{LOAD} will depend on the number of channels, the size of the switches in the multiplexer, the pin capacitance of the multiplexer, if it connects to the outside world, and the input capacitance of the ADC or buffer after the multiplexer.

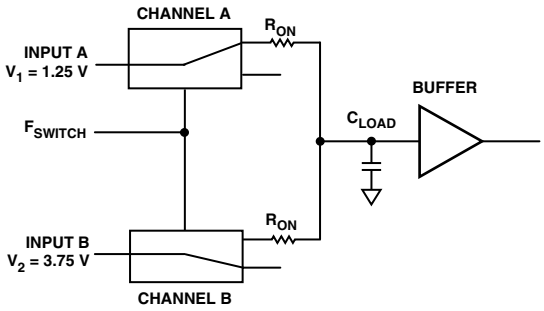

Figure 2. Simplified Multiplexer with Output Capacitance and Two Different Input Voltages

When channel A is selected, C_{LOAD} will charge to V_1. When channel B is selected, C_{LOAD} must charge to V_2. Charging and discharging C_{LOAD} causes a current to flow in both inputs. The actual current flowing will be the usual exponential charging current for a capacitor. However, if a meter is used to measure the current, it will measure the average current, which is given by the formula

$$I = C_{LOAD} \times (V_1 - V_2) \times (F_{SWITCH}/2)$$

The formula contains the term $F_{SWITCH}/2$, since the current flows in either input only half the time. Similarly, if there were eight inputs, then the current in any one input would use the term $F_{SWITCH}/8$. The AD7738 and AD7739 feature over 250 output rates, which can be adjusted on a per channel basis to manage currents due to multiplexing.

If the inputs are low impedance, then these input currents are not a problem. However, for even moderate input impedances, the RC time constant will limit the rate at which switching can occur and still allow C_{LOAD} to settle. On the AD7738 C_{LOAD} = 20 pF and on the AD7739 C_{LOAD} = 10 pF. Both parts automatically allow 7 μs (proportional to clock frequency) for C_{LOAD} to settle after a channel change before conversions start. For 16-bit accuracy, we must ensure $12R_{IN}C_{LOAD} < 7$ μs where R_{IN} is the input impedance including the multiplexer resistance (approximately 100 Ω on the AD7738/AD7739). This suggests

$$R < 29.1\,k\Omega\ (AD7738),\ R < 58\ k\Omega\ (AD7739)$$

If full settling is not achieved, then channel-to-channel isolation will suffer with the output of one channel, depending on the previously converted channel.

A capacitor on the multiplexer input does not cause input leakage due to channel switching since it is permanently connected to one channel. However, in combination with an input impedance, it can average out the previously exponential current due to C_{LOAD}, and this will be discussed later.

CURRENT DUE TO SYSTEM CHOPPING

Chopping is discussed in Analog Devices application note AN-609 (Chopping on Σ-Δ ADCs) and is a technique to reduce offset, offset drift, and improve CMR and PSR. On the AD7738 and AD7739, with chopping enabled, each output consists of two separate conversions.

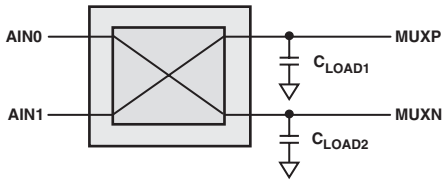

Figure 3. Chopping

For the first conversion, AIN0 connects to MUXP and has to charge C_{LOAD1}, and AIN1 has to charge C_{LOAD2}. For the second conversion, AIN0 connects to MUXN and has to charge C_{LOAD2}, while AIN1 charges C_{LOAD1}. The capacitors for the AD7738 are approximately 20 pF, and for the AD7739 are 10 pF. The average currents will be given by the equation

$$I = 2CVF$$

where *C* is the multiplexer output capacitors, *V* is the differential voltage between V1 AIN0 and AIN1, and *F* is the output rate. The factor of 2 is required because the chop rate is twice the output rate.

The input currents will be exponential in nature and will decay to zero within the allowed 7 μs for low source impedances. However, for higher source impedances or with external RC filters, these currents will cause gain error since the current is proportional to differential input voltage.

Chopping can be disabled by writing a zero to the MSB of the per channel output rate register.

INPUT CURRENT DUE TO SWITCHED CAPACITOR INPUT

The AD7738 and AD7739 feature on-chip buffers. These buffers typically limit input leakage currents to 100 nA and 1 nA, and recommend that you use these buffers. Without buffers, the input to the ADC would look like an 8 pF capacitor (4 pF on the ±2.5 and 0 – 2.5 V ranges), which needs to be recharged at the master clock rate (6.144 MHz max). The input current would be given by

$$I = CVF$$

where *C* is 4 pF or 8 pF, *V* is approximately the analog input voltage minus $A_{VDD}/2$, and *F* is the master clock rate. For an AD7739, this current could average over 100 μA but once again is exponential in nature. If the current has fully settled within one clock cycle, it will cause no errors. Having no errors at the 16-bit level, fully settled means at least 12 RC time constants where *C* is 4 pF or 8 pF as above and *R* is the analog input impedance.

If an external op-amp were used to buffer the inputs, then it would need a gain bandwidth product of at least 8 MHz to keep the impedance low at high frequencies, and a slew rate of around 14 V/μs. However, using the internal buffer to drive the Σ-Δ load, it is then possible to use lower speed buffers to drive the analog inputs as part of a PGA or filtering.

Unbuffered Σ-Δ inputs are still sometimes referred to as high impedance despite the large average current flowing because the current is exponential in nature. When the input is described as being high impedance, it is in fact the input current after the capacitor has been fully charged that is being quoted.

EFFECT OF EXTERNAL RC FILTERS

We have discussed three input current mechanisms, all of which are exponential in nature and will decay to zero if sufficient time is allowed. However, an external RC filter can average these currents to cause dc errors. Taking the input current due to channel hopping as an example:

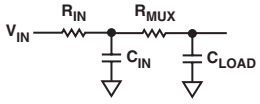

Figure 4. Rectification of Analog Input Currents

In this case, C_{LOAD} is the multiplexer output capacitance, which needs to be charged on every channel change through the multiplexer resistance R_{MUX}. The input filtering will be done using R_{IN} and C_{IN}. When the multiplexer switches, channel C_{IN} needs to be charged and will take its current from the much bigger C_{LOAD}. C_{LOAD} then needs to replace this charge through R_{IN}.

If RC was chosen so that the 3 dB point was at 100 Hz, then the RC time constant is 1.59 ms and the current will take over 19 ms (12 RC time constants) to settle. The resulting voltage drop is approximately R_{IN} C_{LOAD} VF. To keep the voltage error due to this input current small, it is best to achieve the filter cut-off using a small R_{IN} and large C_{IN}.

To further explore this issue, take an extreme case using the AD7739 as an example where C_{IN} = 1 μF, R_{IN} = 100 kΩ, R_{MUX} = 100 Ω, C_{LOAD} = 10 pF, and the AD7739 is running with a channel scanning rate of 800 Hz to give a per channel output rate of 100 Hz. We are allowing a maximum differential input voltage of 2.5 V with common tied to 2.5 V.

Then the input current on any one channel due to multiplexing is given by

$$I = 10^{-12} \times 2.5 \times 100 = 2.5\ nA$$

The maximum current due to chopping is given by

$$I = 10^{-12} \times 2.5 \times 200 = 5\ nA$$

and the buffer input leakage current is 2 nA leading to a total input current of 9.5 nA. The voltage drop across the 100 k resistor is then 950 μV limiting system accuracy to just over 12 bits.

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